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(54) A liquid crystal display device.

(57) The present invention relates to improvements in the frame area of the liquid display panel of a liquid crystal display device, and provides a liquid crystal display device which is enhanced in its blocking ability and the ability of the blocking area to prevent electrostatic failure. A blocking layer 12 is formed in a frame area 1 on TFT array substrate 3. The edge portions of the blocking layer 12 have overlapping areas 14 overlapping the edge portions of each of data lines 10, which are metal layers, with a predetermined overlapping margin d as viewed from a direction perpendicular to the surface of the TFT array substrate 3. An insulation layer 16 is formed on the blocking layer 12 and the TFT array substrate 3. On the insulation layer 16 a semiconductor layer 18 is formed. A plurality of data lines 10 are then disposed on the semiconductor layer 18. The blocking structure thus formed improves the quality of the image display area since it reduces the quantity of light being transmitted from the frame area. Further, the transistor structure formed by the various gate lines, data lines, and blocking lines contributes to the prevention of electrostatic failure.

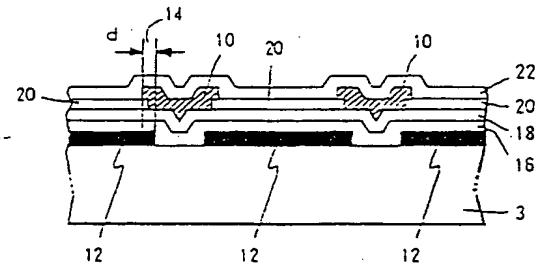

FIG. 3

EP 0 668 526 A2

The present invention is related to liquid crystal display devices, and particularly to improvements in the frame area of the liquid crystal display panel of a liquid crystal display device.

There are various types of conventional liquid crystal display devices available, such as an active matrix liquid crystal display device using thin film transistors (TFTs) as switching elements, and a simple matrix liquid crystal display device of STN and the like. Although these liquid crystal display devices differ in the ways they drive the liquid crystal, they have in common the fact that the liquid crystal is sealed between opposed glass substrates, that signal lines are disposed in a matrix form on the glass substrate, and that the liquid crystals in the vicinity of the intersecting signal lines are driven to construct display pixels.

In addition, the liquid crystal display panel of these conventional liquid crystal display devices has an image display area disposed so as to be exposed in the opening of the case covering the liquid crystal display panel, and a frame area which is the area between the edge portion of the case opening and the periphery or the image display area. The frame area is needed to prevent any part of the image display area being obscured due to the thickness of the case covering the liquid crystal display panel, for instance, when the liquid crystal display area is observed from an oblique angle. The width of the liquid crystal display panel may be about 2 to 3 mm, for instance, for a liquid crystal display device whose image display area is 10 inches in size.

From a signal driver circuit provided outside the frame area, signal lines are disposed in a matrix form over the frame area into the image display area. Since the frame area is an area having no relationship to the image display and the display quality of the liquid crystal display device is degraded if light is transmitted from the frame area, it requires a blocking process.

The conventional blocking process for the frame area is described below.

The most typical method is to form a material having a blocking ability in the frame area on one or both of the opposed glass substrates of the liquid crystal display (LCD) panel. For instance, in most TFT/LCD panels, a blocking layer is formed by depositing a material having a blocking ability, for instance a metal material such as Cr, in the frame area of an opposing substrate having a common electrode formed thereon and opposed to an array substrate having TFTs formed thereon.

However, in this method, the reflection by the blocking layer of the metal material of the opposing substrate is marked, which leads to degradation of the display quality. In addition, it exhibits a further problem in that the manufacturing process of the liquid crystal display device is made more cumbersome due to the need for a blocking layer formation process only for blocking.

In contrast to the above described method which is general, but has problems, a method for blocking the frame area which requires no additional process for forming the blocking layer is disclosed, for instance, in the PUPA 61-32087 official gazette. The blocking methods disclosed in this official gazette and the like are as follows: (1) A blocking area is formed by extending the width of signal lines having a blocking ability passing through the frame area (for instance, metal wirings) to the vicinity of the adjacent signal lines in the frame area, (2) inland-like blocking films are formed between the signal lines in the frame area by the same process as the wiring formation, and, (3) since the lateral wirings and the vertical wirings are formed in a multilayer wiring structure, blocking is performed by forming a blocking layer in which the frame area through which the lateral wirings are passing is paved with the vertical wiring formation material, forming a blocking layer in which the frame area through which the vertical wirings are passing is paved with the lateral wiring formation material. However, in methods (1) and (2), a gap must be left between the wirings and the area to be blocked to prevent short-circuiting between the wirings, and hence there is a problem in that light leaks through this gap and so the blocking ability is incomplete. Further, in method (3), since the overlapping area of the signal lines and the paved blocking layer is large, the stray capacitance is large for the signal lines, which causes a problem in that a signal delay is caused that results in the degradation of the picture quality. In addition, since short-circuiting between the signal lines and the blocking layer is very likely to become a defect fatal to the display panel, the problem of a reduction in the manufacturing yield also occurs.

In an article entitled "Liquid Crystal Display" by T. Fukunaga et al., IBM Technical Disclosure Bulletin, Vol. 36, No. 5, May 1993, pp. 495-496, a method is disclosed in which a blocking layer is formed in a frame area using the wiring material for X-drive lines and Y-drive lines in a manner similar to method (2) described above, and the entire surface of the frame area is coated with a black organic material to increase the blocking ability. However, even this cannot prevent light leakage from the gap in the metal layers, which leads to a problem that higher picture quality cannot be obtained.

In addition, since the frame area is an extra area which has no relationship to the image display as described above, a protection circuit is formed using this area for preventing electrostatic failure which is a problem in the manufacture of the liquid crystal panel. Electrostatic failure and preventive measures against it will now be briefly described. Electrostatic failure is a problem particularly in the TFT/LCD (TFT liquid crystal display device). The gate wirings and the data wirings of a TFT array are electrically insulated by an

insulation layer, and in the manufacturing process of the display panel of a TFT/LCD, they are easily electrostatically charged for various reasons, such as friction from the wind blowing in a clean room, for instance, during a process in the clean room. When the gate lines or data lines are electrostatically charged, a voltage considerably larger than the actual driving voltage is applied to TFTs and the intersections of the wirings, causing dielectric breakdown of the insulation film, and as a result, they cannot function as switching elements or a fatal defect such as a line defect is caused.

Conventionally, to prevent such electrostatic failure, a protection circuit is, for instance, formed as disclosed in the PUPA 63-220289 official gazette. This is characterized in that reference potential wiring is provided and electrically connected to each signal wiring separately by a two-terminal operation switching element. This necessarily occupies a large area dedicated to the protection circuit so that the switching element has an appropriate resistance value as a protection circuit. In a circuit of this type, to prevent reduction in the manufacturing yield such as short-circuiting of the wirings, it is necessary to maintain the gap of the metal layer in the vicinity of the protection circuit, conflicting with the blocking ability. Thus it cannot be formed in the frame area unless there is a blocking layer on the opposing substrate side. In consequence, this circuit must be formed outside the frame area, but it is usually difficult for various reasons to acquire such area outside the frame area.

In the protection circuit disclosed in the PUPA 62-65455 official gazette, adjacent wirings in the frame area are electrically short-circuited by a high-resistance connector. This high-resistance connector can be formed in the frame area. However, since the high-resistance connector constituting the circuit has substantially linear current-voltage characteristics, the display quality is reduced by the interaction between the signal lines if the resistance value is decreased, and the capability of preventing electrostatic failure becomes smaller. Consequently, there is a problem in that the display screen quality and the prevention of electrostatic failure become incompatible with each other.

As described above, conventional liquid crystal display devices have various problems to be solved relating to the blocking ability of the frame area, and the ability to prevent electrostatic failure in the protection circuit formed in the frame area.

Accordingly, it is an object of the present invention to provide a liquid crystal display device in which the blocking ability of the frame area around an image display area is increased without causing a large signal delay and the like in signal wirings. Preferably, the present invention should further provide a liquid crystal display device in which the ability to prevent electrostatic failure is increased.

Accordingly the present invention provides a liquid crystal display device comprising: a transparent substrate having a frame area defined around an image display area; a wiring layer consisting of a plurality of metal wirings extracted over said frame area from said image display area and formed at predetermined intervals; a plurality of first metal layers formed between said adjacent metal wirings and separated from said adjacent metal wirings by an insulation layer, the first metal layers having edge portions overlapping edge portions of each of said plurality of metal wirings by a predetermined overlapping margin as viewed from a direction perpendicular to the surface of said transparent substrate.

The present invention provides a liquid crystal display device comprising a transparent substrate having a frame area defined around an image display area, and a wiring layer consisting of a plurality of metal wirings extracted over the frame area from the image display area and formed at predetermined intervals. An insulation layer is typically formed on the wiring layer, and a plurality of island-like metal layers are then formed on the insulation layer between the adjacent metal wirings. These metal layers have edge portions overlapping the edge portions of each of the plurality of metal wirings by a predetermined overlapping margin as viewed from a direction perpendicular to the surface of the transparent substrate.

In preferred embodiments a semiconductor layer is formed on the insulation layer so as to electrically contact the plurality of metal wirings. A transistor structure is thereby formed which contributes to the prevention of electrostatic failure.

In preferred embodiments, the plurality of metal wirings are either data lines or gate lines, and the plurality of metal layers are formed out of the metal forming either of the data lines or gate lines.

Further, in preferred embodiments, the plurality of metal wirings in said wiring layer are formed at first intervals, and the plurality of first metal layers are formed in said frame area at second intervals between said adjacent metal wirings, the liquid crystal display device further comprising: a plurality of second metal layers formed on said insulation layer so as to connect to each of said plurality of metal wirings, and having edge portions overlapping the edge portions of each of said first metal layers by a predetermined overlapping margin as viewed from a direction perpendicular to the surface of said transparent substrate; the semiconductor layer formed on said insulation layer electrically contacting said plurality of second metal layers.

Preferably, the second metal layers are formed out of the metal forming either the data lines or gate lines.

The overlapping margin is generally chosen to have a width which is substantially identical to the overlapping precision in the manufacturing process.

Further, a layer of a black organic material is preferably added to the frame area.

In preferred embodiments, a liquid crystal display device is produced in which the blocking ability of the frame area and the ability to prevent electrostatic failure are increased without increasing the manufacturing process.

In accordance with the preferred embodiment of the present invention, since a plurality of island-like metal layers are formed in a frame area, which island-like metal layers have edge portions overlapping the edge portions of metal wirings through an insulation layer with a predetermined overlapping margin as viewed from a direction perpendicular to the surface of a transparent substrate, light being transmitted through the transparent substrate can be intercepted in the frame area by the overlapping metal wirings and metal layers.

Further, in accordance with preferred embodiments of the present invention, in the frame area, a semiconductor layer is formed on the wiring layer, the insulation layer is formed on the semiconductor layer, and the metal layers are formed on the insulation layer between the plurality of metal wirings of the wiring layer. Thus a transistor is formed in which a metal layer is used as the gate and adjacent metal wirings are used as the source or drain, whereby a circuit can be constructed in the frame area, which circuit has non linear current-voltage characteristics such that little current flows when a low voltage is applied and a large current flows when a high voltage is applied. A protection circuit can thus be formed for blocking the frame area and preventing electrostatic failure.

The present invention will be described further, by way of example only, with reference to an embodiment thereof as illustrated in the accompanying drawings, in which:

Figure 1 shows a liquid crystal display device according to an embodiment of the present invention;

Figure 2 is a partial enlarged view of the frame area of the liquid crystal display device according to an embodiment of the present invention;

Figure 3 is a partial sectional view of the frame area of the liquid crystal display device according to an embodiment of the present invention;

Figure 4 is a partial enlarged view of the frame area of the liquid crystal display device according to an embodiment of the present invention;

Figure 5 is a partial sectional view of the frame area of the liquid crystal display device according to an embodiment of the present invention; and

Figure 6 is a circuit diagram showing the protection circuit of the liquid crystal display device according to an embodiment of the present invention.

A liquid crystal display device according to one embodiment of the present invention is described with reference to Figures 1 to 6.

First, the construction of the liquid crystal display device of this embodiment is described using Figures 1 to 5. The liquid crystal display device used in this embodiment is a TFT/LCD. Figure 1 shows the liquid crystal display panel 8 of the liquid crystal display device of this embodiment. A rectangular image display area 2 having a screen size of, for instance, 10 inches, is disposed in the center of a TFT array substrate 3 which is a transparent substrate. A frame area 1 having a width of the order of 2 to 3 mm is provided between the outer periphery of the image display area 2 and the periphery of the TFT array substrate 3.

Although not shown, a plurality of gate lines are formed from the peripheral portion of the TFT array substrate 3 into the image display area 2 passing over the frame area 1 laterally in Figure 1. Further, a plurality of data lines are formed from the peripheral portion of the TFT array substrate 3 into the image display area 2 passing over the frame area 1 vertically in Figure 1. In the intersection areas of the data lines and the gate lines, TFTs, display electrodes, and the like are disposed to form display pixels.

Through a seal material (not shown) formed in proximity to the boundary of the frame area 1 and the peripheral portion of the TFT array substrate 3, an opposing electrode substrate 5, which is a transparent electrode substrate, is disposed at a position opposed to the TFT array substrate 3. Liquid crystal is sealed between the TFT array substrate 3 and the opposing electrode substrate 5. In addition, the liquid crystal display device of this embodiment employs a transmission type display device in which light is transmitted from the back of the TFT array substrate 3 to the element side, but may employ one in which light is transmitted from the element side to the back to the substrate.

The structure of the frame area of the liquid crystal display device of this embodiment is described in detail using Figures 2 and 3. Figure 2 shows an enlargement of a part 4 of the frame area 1 in Figure 1. The part 4 of the frame area 1 is an area through which data lines are passing. Figure 3 is a cross-sectional view along the A-A cross section of Figure 2. The opposing electrode substrate 5 is omitted in Figure 3.

On the frame area 1 of the TFT array substrate 3 is formed a blocking layer 12 having a thickness of, for instance, about 0.3 μm. The material forming the blocking layer 12 is, for instance, a Mo alloy, Ta, Cr, Al, and the like, and preferably the metal forming the gate line is used. By using the metal forming the gate line, the blocking layer 12 can be formed in the manufacturing process simultaneously with the formation of the gate lines.

The shape arrangement of the blocking layer 12 is predetermined on the basis of the positional relationship of a plurality of data lines 10 (formed in a

process after the blocking layer 12) to be described later. The blocking layer 12 is formed in the shape of islands in the frame area 1. The edge portions of the shield layer 12 have overlapping areas 14 overlapping the edge portions of each of the data lines 10, which are metal layers, with a predetermined overlapping margin, d, as viewed from a direction perpendicular to the surface of the TFT array substrate 3. The predetermined overlapping margin, d, preferably has a width which is substantially identical to the overlapping precision in the manufacturing process. If overlapping margin d is smaller than the overlapping precision, a gap may occur in the area to be blocked. In this embodiment, as shown in Figure 2, since the individual data lines 10 are extending in the frame area 1 toward the peripheral portion of the TFT array substrate 3 so that the spacing between them becomes narrower, the blocking layer 12 is shaped in a parallelogram or trapezoid. However, the blocking layer 12 needs only to be shaped so that it overlaps along the shape of the edge portions of each data line 10 in the frame area with a predetermined overlapping margin. In the frame area 1, the width of the data lines 10 is about 20 to 40 μm, and the spacing between the data lines 10 is about 20 to 100 μm. Overlapping margin d is about 1 to 10 μm, and the width of the blocking layer 12 in the direction substantially perpendicular to the data lines 10 is about 30 to 120 μm in the center, with the width in the direction substantially parallel with the data lines 10 being about 2 to 5 mm.

On the blocking layer 12 and the TFT array substrate 3, an insulation layer 16 is formed with a thickness of, for instance, about 0.4 μm. The insulation layer 16 can, for instance, be a Si oxide film, Si nitride film, and the like, and preferably the material forming the gate insulation film of the TFT array formed in the image display area 2 is used. By using the material forming the gate insulation film, the insulation film 16 can be formed in the manufacturing process simultaneously with the formation of the gate insulation film of the TFT.

On the insulation film 16, a semiconductor layer 18 is formed having a thickness of, for instance, about 500 Å. The material forming the semiconductor layer 18 is, for instance, amorphous silicon (a-Si) and preferably is the material forming the channel region of the TFT array formed in the image display area 2. By using the material forming the channel region, the semiconductor layer 18 can be formed in the manufacturing process simultaneously with the formation of the channel region of the TFT.

The plurality of data lines 10 formed in the image display area 2 are disposed on the semiconductor layer 18 in the frame area 1, and extend so as to connect to a data line driver circuit (not shown) formed in the periphery of the TFT array substrate 3. Although not shown, a P-doped a-Si layer having a thickness of about 500 Å is preferably formed between the semiconductor layer 18 of a-Si and the data lines 10. Further, etching stopper layers 20 are formed between the data lines 10 on the semiconductor layer 18. On the data lines 10 and the etching stopper layers 20 a passivation layer 22 is formed. These layers can also be formed simultaneously with the formation of the TFT array, and this is preferable.

The structure of the frame area 1 of the liquid crystal display device of this embodiment will now be described in detail using Figures 4 and 5. Figure 4 is an enlargement of a part 6 of the frame area 1 in Figure 1. The part 6 of the frame area 1 is an area through which the gate lines are passing. Figure 5 is a cross-sectional view along the B-B cross section of Figure 4. In Figure 5, the opposing electrode substrate 5 is omitted.

A plurality gate lines 24, which are about 0.3 μm thick, about 20 to 100 μm wide, and formed out of a Mo alloy, Ta, Cr, Al, and the like, pass over the frame area 1 on the TFT array substrate 3. The distance between the gate lines 24 is about 50 to 200 μm. Between the gate lines 24 of the frame area 1, a blocking layer 26 in the shape of islands is formed out of the material forming the gate line simultaneously with the formation of the gate lines. The thickness and width of the blocking layer 26 are substantially the same as those of the gate lines, and the spacing between the blocking layer 26 and the gate line 24 may be about 10 to 50 μm, which prevents short-circuiting between the two. The metal forming the gate line is preferably used as the material forming the shield layer 26. By using the metal forming the gate line as described above, the blocking layer 26 can be formed simultaneously with the formation of the gate lines in the manufacturing process.

An insulation layer 16 is formed on the gate lines 24 in the frame area 1, the blocking layer 26, and the TFT array substrate 3.

A blocking layer 30 is formed on the insulation layer 16 on the gate line 24 in the frame area 1. The blocking layer 30 and the gate line 24 are electrically connected by a through-hole 28 provided in the insulation layer 16. The material forming the blocking layer 30 is, for instance, Al, Mo, Cr, and the like, and the metal forming the data lines 10 is preferably used. By using the metal forming the data line, the blocking layer 30 can be formed simultaneously with the formation of the data lines 10 in the manufacturing process.

The shape and arrangement of the blocking layer 30 is determined in regard to the shape and position of the plurality of blocking layers 26. The blocking layer 30 is formed in the shape of islands. The edge portions of the blocking layer 30 has overlapping areas 32 overlapping the edge portions of the blocking layer 26, which is a metal layer, with predetermined overlapping margin d as viewed from a direction perpendicular to the surface of the TFT array substrate 3. Predetermined overlapping margin d preferably has a

width which is substantially identical to the overlapping precision in the manufacturing process, as described above. In this embodiment, as shown in Figure 4, each gate line 24 extends in the frame area 1 toward the periphery of the TFT array substrate 3 at a little angle with the width direction of the frame area 1, and thus the shape of the blocking layers 26 and 30 is parallelogram of trapezoid, though the blocking layers 26 and 30 may be shaped so that they are overlapping each other with a predetermined overlapping margin along the edge portions of each gate lines 24 in the frame area 1. Overlapping margin d of the overlapping area 32 is about 1 to 10 μm, the width of the blocking layer 26 in a direction substantially perpendicular to the gate lines 24 is about 10 to 100 μm, and the width in a direction substantially parallel with the gate lines 24 is about 2 to 5 mm. The width of the blocking layer 30 in a direction substantially perpendicular to the gate lines 24 is about 50 to 150 μm, and the length in a direction substantially parallel with the gate lines 24 is about 2 to 5 mm.

On the insulation layer 16 and between the shield layers 30, a semiconductor layer 18 contacting the blocking layers 30 is formed, and an etching stopper layer 20 is formed thereon.

A passivation layer 22 is formed on the blocking layers 30 and the etching stopper layer 20.

In the frame area 1 over which the signal lines such as the data lines 10 or the gate lines 24 do not pass, for instance, on the right side of the frame area in Figure 1, the metal for forming the data lines 10 or gate lines 24 may be deposited to form a blocking layer simultaneously with the formation of these wirings, or a structure in which the two metal layers overlap each other with a predetermined precision may be provided everywhere.

The blocking function of the frame area of the liquid crystal display device of this embodiment will now be described.

As shown in Figures 2 to 5, in accordance with the liquid crystal display device of the preferred embodiment of the present invention, the data lines and the blocking layer (Figures 2 and 3) or the blocking layers (Figures 4 and 5) overlap each other in the frame area, and thus leakage light passing through the frame area can be nearly completely intercepted.

In addition, since the overlapping area 14 for the data lines 10 (which are metal wirings) and the blocking layer 12 (formed out of a metal material), and the overlapping area 32 for the metal blocking layer 30 connected to the gate lines 24 (which are metal wirings) and the blocking layer 26 (formed out of a metal material) may have a width substantially identical to the overlapping precision for the pattern formation, the signal delay in the signal lines such as the data lines 10 and the gate lines 24 can be controlled to be minimum. In consequence, in accordance with the liquid crystal display device of the embodiment, the effect on the display quality by the signal delay can be ignored. Further, as shown in Figures 4 and 5, since the blocking layer 30 is a metal layer which is superposed on the gate line 24 (signal wiring) so as to be electrically connected to and in parallel with the gate line 24, it functions to reduce the resistance value of the gate line 24. Accordingly, the structure of the blocking layer 30 functions to further decrease the signal delay in the gate line 24.

Further, in such a structure as this embodiment, even if the two metal layers overlapping each other in the frame area 1, for instance the blocking layer 12 and the two data lines 10 adjacent to the blocking layer 12, break through the insulation layer 16 and short-circuit, the redundancy is such that no practical problem occurs as long as the short-circuiting occurs between one island-like layer 12 and one of the data lines 10 adjacent to that island-like layer 12. Therefore, no problem occurs, either, in the manufacturing yield. This also applies to the blocking layers 30 and 26 connected to the gate lines 24.

Thus, in accordance with this embodiment, the whole frame area required to be blocked can fully be blocked without causing a large signal delay in the signal lines.

The function of preventing electrostatic failure in the liquid crystal display device of this embodiment will now be described.

The blocking structure of the frame area 1 shown in Figure 3 has a transistor structure as described below. That is, on the TFT array substrate 3, the blocking layer 12 functioning as the gate of a transistor is formed, and the insulation layer 16 functioning as a gate insulation film is formed thereon. The semiconductor layer 18 functioning as a channel is formed on the insulation layer 16 on the blocking layer 12 (which is the gate). The semiconductor layer 18 is connected to two data lines 10 functioning as a source electrode or drain electrode through n^+-a-Si (not shown). This transistor structure is repeatedly formed in a series on the upper and lower sides of the frame area 1 shown in Figure 1, forming the protection circuit of this embodiment.

Further, the blocking structure of the frame area 1 shown in Figure 5 forms the following transistor structure. That is, on the TFT array substrate 3 is formed the blocking layer 26 functioning as the gate of a transistor. The two gate lines 24 formed on the TFT array substrate 3 on both sides of the blocking layer 26 are electrically connected to the upper layer thereof, and construct a source electrode or drain electrode along with the blocking layer 30 having edge portions which overlap the edge portions of the blocking layer 26 with a predetermined overlapping margin as viewed from a direction perpendicular to the surface of the TFT array substrate 3. On the blocking layer 26 (acting as the gate) is formed the semiconductor layer 18 through the insulation layer

16 functioning as a gate insulation film. The semiconductor layer 18 is connected to the blocking layers 30 which are the source-drain electrodes, and functions as a channel. This transistor structure is repeatedly formed on the left side of the frame area 1 shown in Figure 1, forming the protection circuit of this embodiment.

Although the protection circuits formed on the upper, left, and lower sides of the frame area 1 are electrically connected to each other in this embodiment, this is not essential and the protection circuit on each side may be independent. The protection circuit formed in the frame area 1 is described using Figure 6. Figure 6 shows a corner portion of the frame area 1 at the upper left of the liquid display panel 8 shown in Figure 1. In Figure 6, the plurality of data lines 10 of the figure are disposed vertically over the frame area 1 into the image display area 2. Further, the plurality of gate lines 24 of the figure are disposed laterally over the frame area 1 into the image display area 2 through the insulation layer 16 (not shown) and orthogonal to the data lines 10. Pixel areas 36 are formed in the intersection portions of the data lines 10 and the gate lines 24 in the image display area 2. In the pixel area 36 is formed a TFT which has the drain electrode, not shown, connected to the data line 10, the gate electrode connected to the gate line 24, and the source electrode, also now shown, connected to the display electrode.

In the frame area 1 in Figure 6, each data line 10 is connected to the source/drain electrode of the transistor 38 formed between the data lines 10. In addition, the gate electrode of the transistor 38 is capacitance-coupled to the data lines 10 on both sides. Each gate lines 24 is also connected to the source/drain electrode of the transistor 38 formed between the gate lines 24. In addition, the gate electrode of the transistor 38 is capacitance-coupled to the gate lines 24 on both sides.

The gate electrode of this transistor 38 is the blocking layer 12 shown in Figure 3 or the blocking layer 26 shown in Figure 5.

The protection circuit formed in the frame area 1 according to this embodiment has a structure in which a switching element is formed between each data line 10 and each gate line 24, which element has a nonlinear current-voltage characteristic such that little current flows at a low voltage, but a large current flows when a high voltage is applied.

In the manufacturing process of a liquid crystal display device, if static electricity large enough to cause a failure occurs either in the data line 10 or gate line 24, a large potential difference is also produced between the capacitance-coupled blocking layer 12 or 26 (functioning as the gate in the transistor 38) by a large potential difference caused between the adjacent signal lines (data lines 10 or gate lines 24), and as a result, a large current flows in the semiconductor layer 18 of the protection circuit. This has the effect of reducing the potential difference between the adjacent wirings due to the produced static electricity to the threshold voltage of the transistor 38 constituting the protection circuit, whereby electrostatic failure can be prevented. A large current can be made to flow in the semiconductor layer 18 because the width of the blocking layer 12 or 26 as the gate can be equal to the width of the frame area 1, or about 3 mm, and thus an extremely long channel width can be obtained.

Thus, the prevention of electrostatic failure according to this embodiment is achieved by the protection circuits formed in the frame area 1 and comprising switching elements having nonlinear current-voltage characteristics.

On the one hand, since substantially the entire frame area 1 can be utilized as a protection circuit for preventing electrostatic failure, electrostatic failure can be effectively prevented without reduction in manufacturing yield or display quality due to the protection circuit.

On the other hand, with the signal voltage (drive voltage) level for image display control, the potential difference between the blocking layer 12 functioning as the gate of a transistor by capacitive coupling with the data lines 10 and the data lines 10 is no more than the signal voltage amplitude and lower than the threshold voltage of the transistor 38 forming a protection circuit. Thus little current flows in the semiconductor layer 18 of the protection circuit, whereby a high screen quality can be maintained in the image display. Similarly to the scanning voltage (drive voltage) level for image display control, the potential difference between the blocking layer 26 functioning as the gate of a transistor by capacitive coupling with the gate lines 24 and the gate lines 24 is about half the potential difference between the ON and OFF states of the scan signal, and it exceeds the threshold voltage of the transistor 38 forming the protection circuit so as to turn on the transistor 38. However the effect on the scan signal by the current flowing in the semiconductor layer 18 of the protection circuit is negligible, so that a high quality screen can be maintained in the image display.

In addition, the wiring for supplying the potential of each pixel for stored capacity or the wiring for supplying the potential of the opposing electrode can be connected to the protection circuit shown in Figure 6 in a manner similar to this embodiment for protection against electrostatic failure.

Thus, the frame area 1 in this embodiment has a structure which combines the blocking of the frame area 1 and the protection circuit for preventing electrostatic failure. In accordance with this embodiment, a liquid crystal display device can be implemented in which a protection circuit need not be provided outside the frame area as was done in the prior art, and

the interaction between wiring signals can be ignored.

The present invention is not restricted to the above described embodiment, but various modifications can be made to it.

For instance, although in the above embodiment a protection circuit is formed in the frame area 1 both for blocking the frame area 1 and preventing electrostatic failure, one may choose to provide only the blocking function without forming the semiconductor layer 18 of the frame area 1.

In addition, in the above embodiment as shown in Figures 3 and 5, the blocking layer 12, the insulation layer 16, the semiconductor layer 18, and the data lines 10 are formed on the TFT array substrate 3 in this order, and hence the gate lines 24 and the blocking layer 26, the insulation layer 16, the semiconductor layer 18, and the blocking layer 30 are formed in this order, but they may be formed in a reverse placement order for correspondence to the structure of the TFT formed in each pixel 36. That is, on the TFT array substrate 3, the data lines 10, the semiconductor layer 18, the insulation layer 16, and the blocking layer 12 may be formed in this order, and the blocking layer 30, the semiconductor 18, the insulation layer 16, and the gate lines 24, and the blocking layer 26 may be formed in this order.

Furthermore, it is, of course, possible that the data lines 10 shown in Figure 3 are changed to gate lines or the gate lines 24 shown in Figure 5 are changed to data lines, depending on the structure of the TFT to be formed.

In addition, to make the blocking effect more complete, a blocking layer made of a black organic material may be added above the frame area 1 of the TFT array substrate 3. Since this blocking layer can be formed for blocking between each pixel 36 in the image display area 2 simultaneously with the formation of a black matrix of the black organic material on the TFT array substrate 3 side, the blocking ability for the frame area 1 can be further improved without increasing the number of manufacturing process steps.

Further, although the present invention is applied to a TFT/LCD in the above described embodiment, it is, of course, not limited to that but is applicable to the blocking of the frame area of a display device in which the wirings are formed in a matrix form.

In addition, although the present invention has been described with respect to a transmission display device in the above embodiment, it is to be understood that it is not limited to that, but applicable to the frame area of a reflection display device.

In accordance with the described embodiment of the present invention, the blocking and prevention of electrostatic failure for the frame area of the display panel in a liquid crystal display device can be simultaneously and effectively achieved, without increasing the number of manufacturing process steps.

Claims

1. A liquid crystal display device comprising:

   a transparent substrate (3) having a frame area (1) defined around an image display area (2);

   a wiring layer consisting of a plurality of metal wirings (10; 24, 30) extracted over said frame area (1) from said image display area (2) and formed at predetermined intervals;

   a plurality of first metal layers (12; 26) formed between said adjacent metal wirings (10; 24, 30) and separated from said adjacent metal wirings (10; 24, 30) by an insulation layer (16), the first metal layers (12; 26) having edge portions overlapping edge portions of each of said plurality of metal wirings by a predetermined overlapping margin (14; 32) as viewed from a direction perpendicular to the surface of said transparent substrate (3).

2. A liquid crystal display device as claimed in claim 1, further comprising a semiconductor layer (18) formed on said insulation layer (16) so as to electrically contact said plurality of metal wirings (10; 24, 30).

3. A liquid crystal display device as claimed in claim 1 or 2, wherein said plurality of metal wirings are either data lines (10) or gate lines (24), and said plurality of first metal layers (12; 26) are formed out of the metal forming either of said data lines (10) or said gate lines (24).

4. A liquid crystal display device as claimed in claim 2 or claim 3, wherein the plurality of metal wirings (24) in said wiring layer are formed at first intervals, and the plurality of first metal layers (26) are formed in said frame area (1) at second intervals between said adjacent metal wirings (24), the liquid crystal display device further comprising:

   a plurality of second metal layers (30) formed on said insulation layer (16) so as to connect to each of said plurality of metal wirings (24), and having edge portions overlapping the edge portions of each of said first metal layers (26) by a predetermined overlapping margin as viewed from a direction perpendicular to the surface of said transparent substrate (3);

   the semiconductor layer (18) formed on said insulation layer electrically contacting said plurality of second metal layers (30).

5. A liquid crystal display device as claimed in claim 4 wherein said second metal layers (30) are formed out of the metal forming either said data lines (10) or said gate lines (24).

6. A liquid crystal display device as claimed in any preceding claim, wherein said overlapping margin has a width which is substantially identical to the overlapping precision in the manufacturing process.

7. A liquid crystal display device as claimed in any preceding claim, wherein a layer of a black organic material is added to said frame area (1).

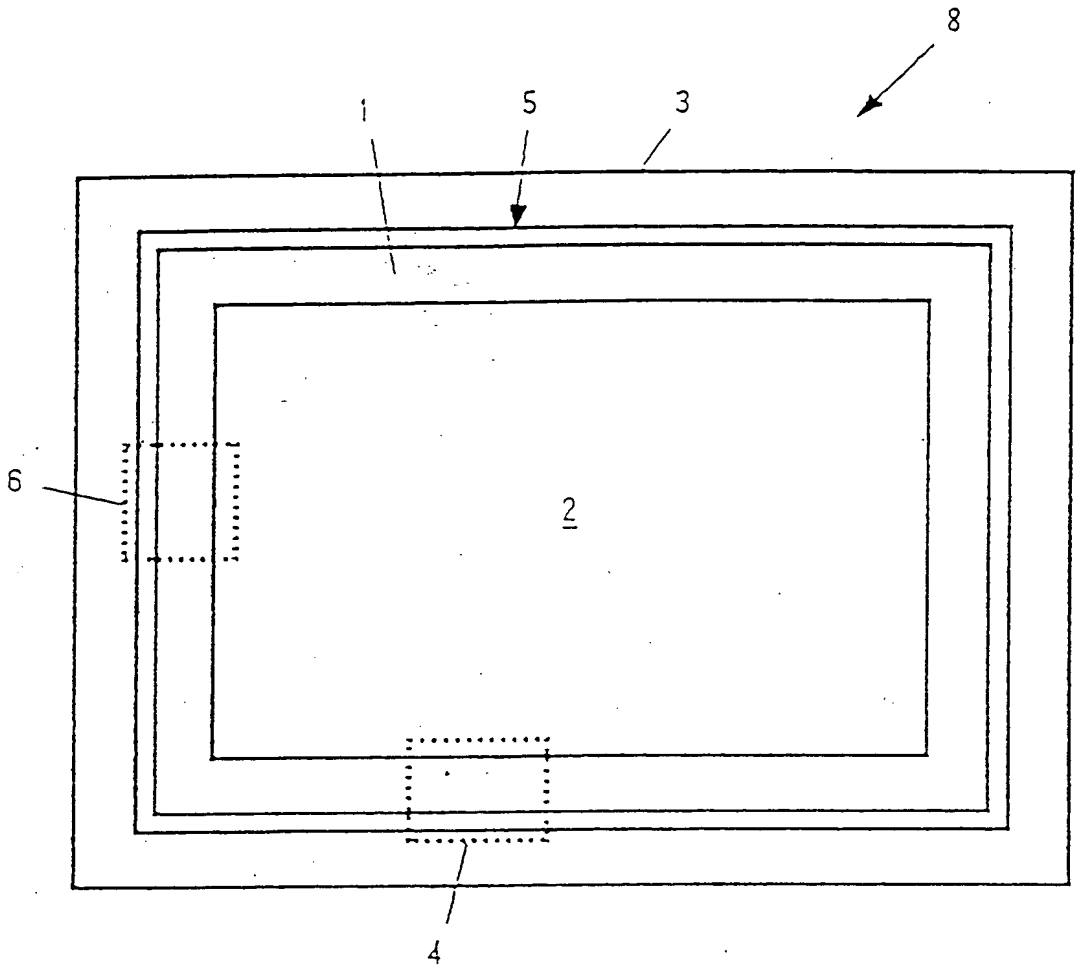

FIG. 1

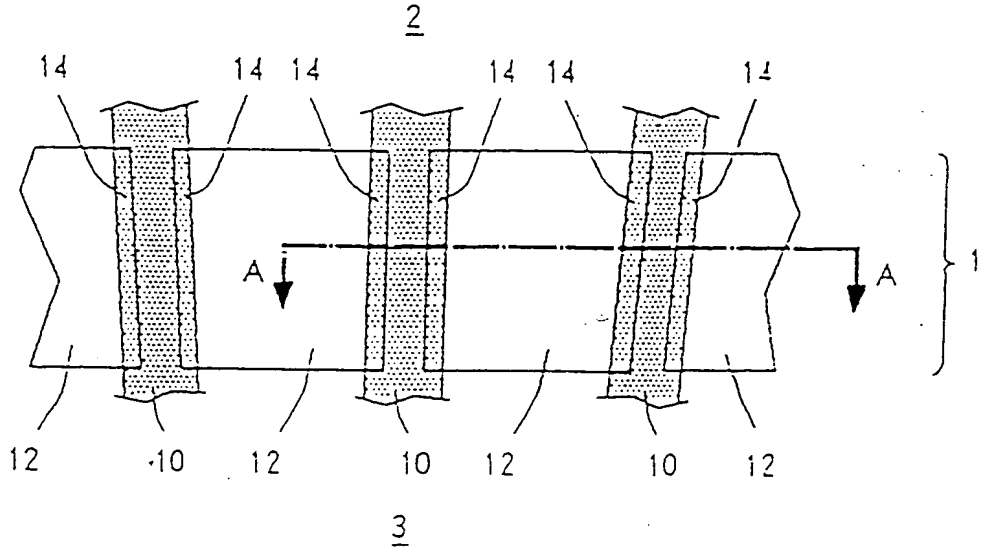
2
14
14
14
14
14
14
A
A
1
12
10
12
10
12
10
12
3

FIG. 2

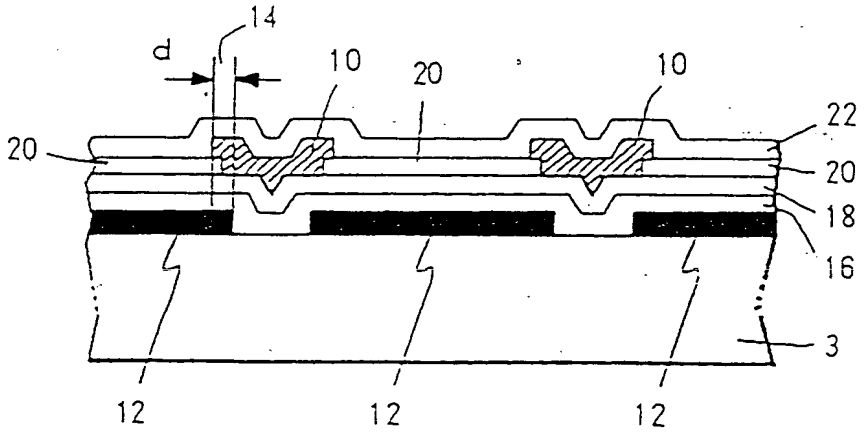
14
d
10
20
10
22
20
20
18
16
3
12
12
12

FIG. 3

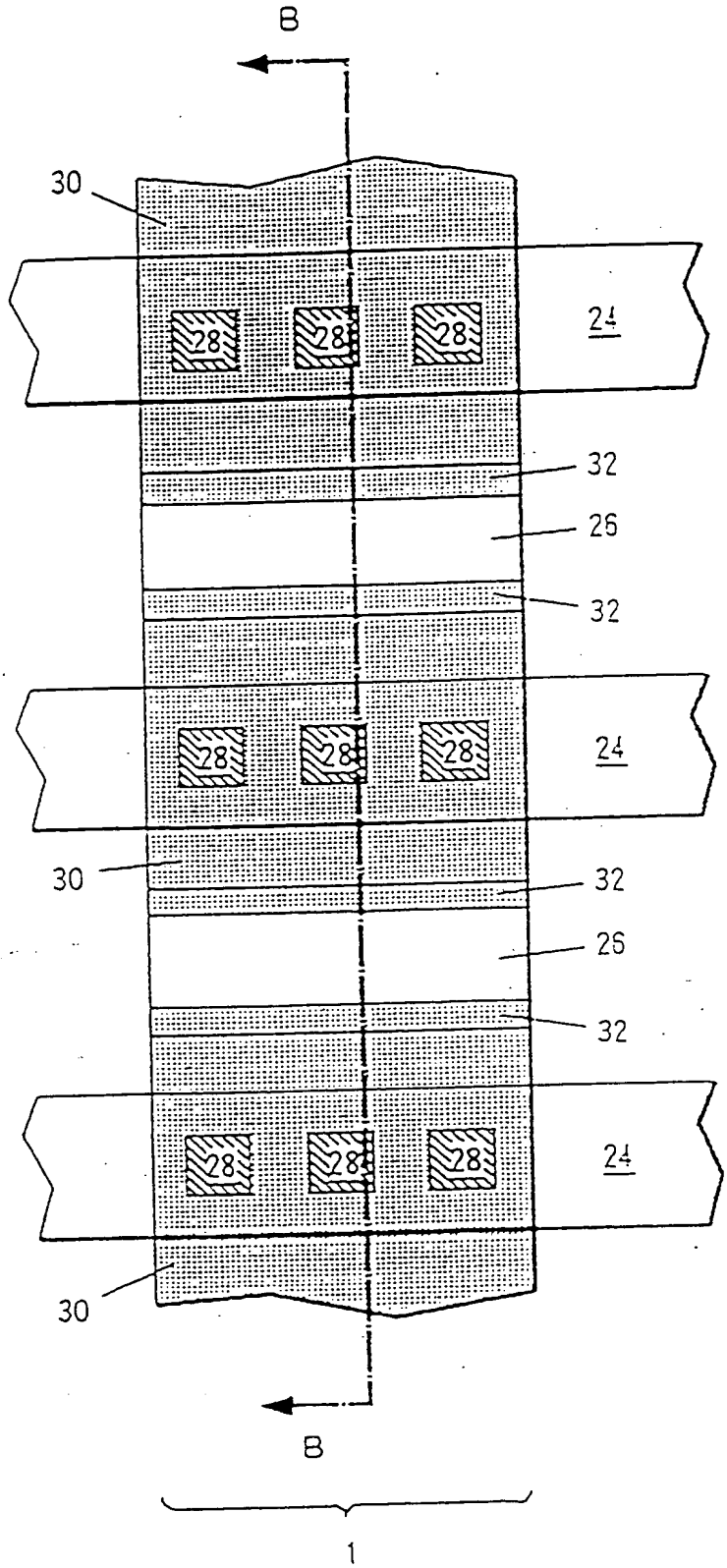

FIG. 4

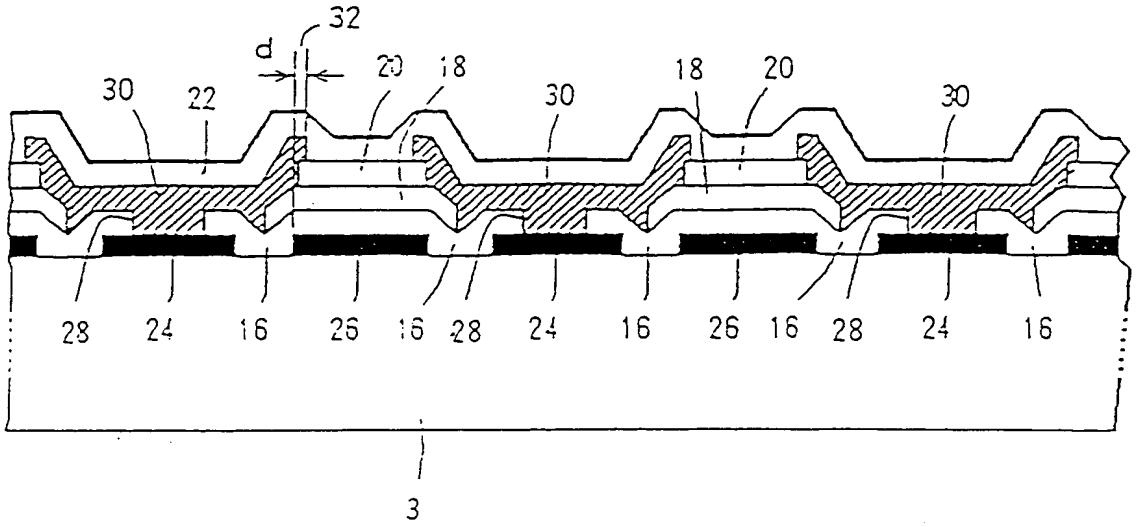
32
d
30
22
20
18
30
18
20
30
28
24
16
26
16
28
24
16
26
16
28
24
16
3

FIG. 5

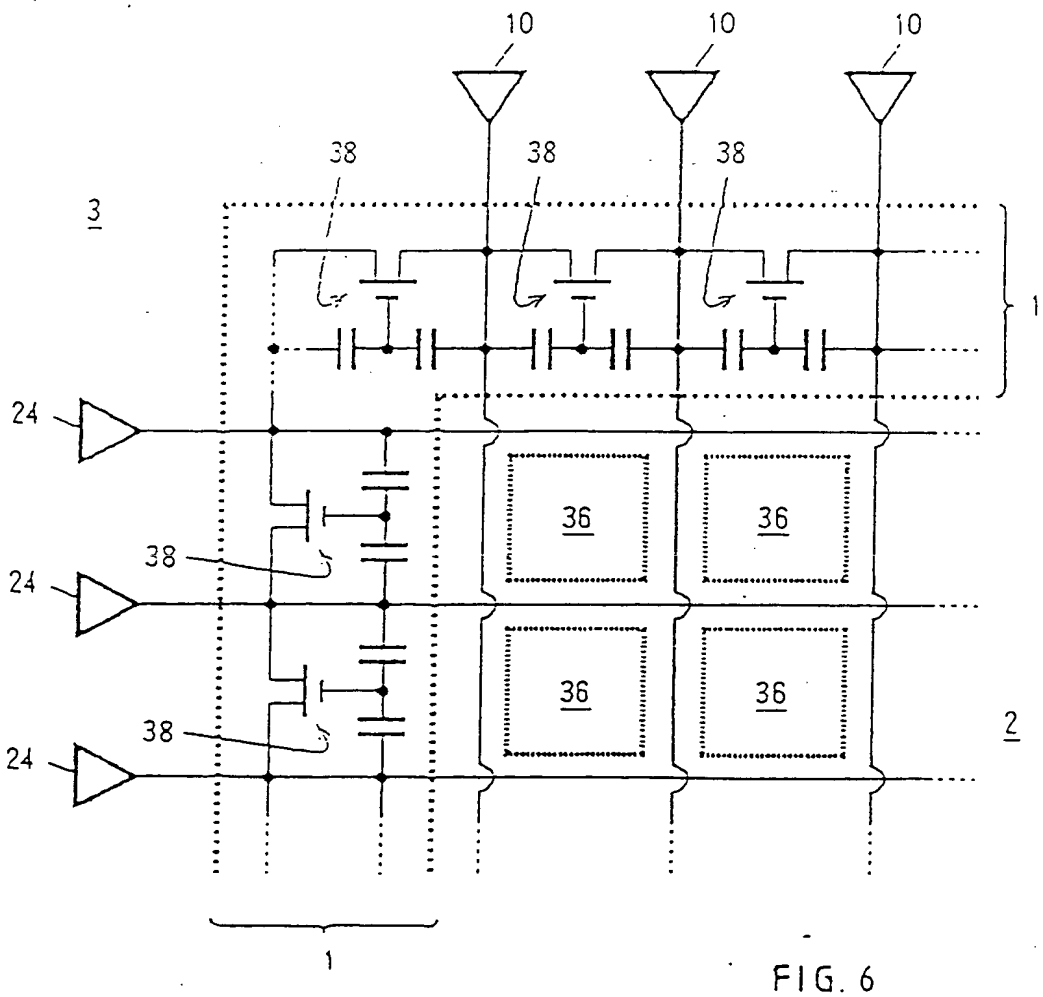
10
10
10
38
38
38
3
1
24
36
36
38
24
36
36
38
24
2
1

FIG. 6

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(54) A liquid crystal display device

(57) The present invention relates to improvements in the frame area of the liquid display panel of a liquid crystal display device, and provides a liquid crystal display device which is enhanced in its blocking ability and the ability of the blocking area to prevent electrostatic failure. A blocking layer (12) is formed in a frame area (1) on TFT array substrate (3). The edge portions of the blocking layer (12) have overlapping areas (14) overlapping the edge portions of each of data lines (10), which are metal layers, with a predetermined overlapping margin d as viewed from a direction perpendicular to the surface of the TFT array substrate (3). An insulation layer (16) is formed on the blocking layer (12) and the TFT array substrate (3). On the insulation layer (16) a semiconductor layer (18) is formed. A plurality of data lines (10) are then disposed on the semiconductor layer (18). The blocking structure thus formed improves the quality of the image display area since it reduces the quantity of light being transmitted from the frame area. Further, the transistor structure formed by the various gate lines, data lines, and blocking lines contributes to the prevention of electrostatic failure.

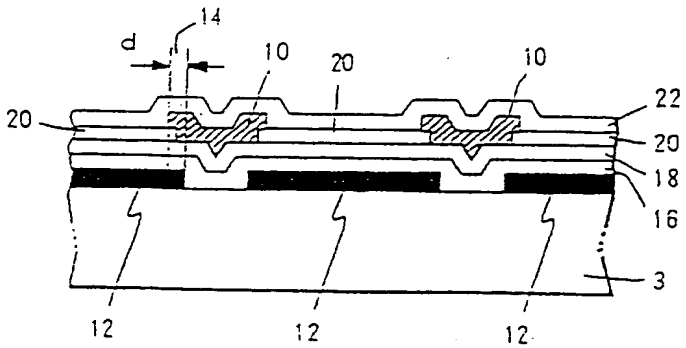

FIG. 3

EP 0 668 526 A3

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EUROPEAN SEARCH REPORT

Application Number
EP 95 30 0418

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 36, no. 5, 1 May 1993 page 495/496 XP 000409074 'LIQUID CRYSTAL DISPLAY' * the whole document *	1,3,7	G02F1/1335 G02F1/136
A	EP-A-0 556 989 (TOKYO SHIBAURA ELECTRIC , IBM) 25 August 1993 * column 14, paragraph 1 - paragraph 2 * * column 16, paragraph 5 - paragraph 6; figures 21,27,29 *	1,2	
A	PATENT ABSTRACTS OF JAPAN vol. 017 no. 512 (P-1613) ,14 September 1993 & JP-A-05 134240 (OPTREX CORP) 28 May 1993, * abstract *	1,7	
D,A	PATENT ABSTRACTS OF JAPAN vol. 011 no. 254 (E-533) ,18 August 1987 & JP-A-62 065455 (TOSHIBA CORP) 24 March 1987, * abstract *	1,2	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

G02F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 March 1996	Wongel, H

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